REMARKS

The Office Action mailed on August 9, 2001, has been received and reviewed. Claims 1-46, 69-74, and 91-109 have been withdrawn from consideration as being drawn to a nonelected invention. Each of claims 1-46, 69-74, and 91-109 has, therefore, been canceled without prejudice or disclaimer. Claims 47-68 and 75-90 are currently pending and under consideration in the above-referenced application. Claims 47-68 and 75-90 stand rejected.

Reconsideration of the above-referenced application is respectfully requested.

Drawings

The drawings were objected to under 37 C.F.R. § 1.83(a) for not illustrating a dielectric layer on an active surface of a semiconductor die, as described in the specification. It is respectfully submitted that the drawings already illustrate such a dielectric layer. For example, FIGs. 8 and 9 both depict a semiconductor device 10 with a dielectric layer 42 on an active surface thereof. Accordingly, withdrawal of the objection to the drawings is respectfully requested.

Rejections Under 35 U.S.C. § 103(a)

Kepchar

Claims 47-68 and 75-90 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 4,138,672 to Kepchar (hereinafter "Kepchar").

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on

applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Kepchar teaches and illustrates (*e.g.,* in FIG. 1 thereof) a method and apparatus for connecting a light-emitting diode (LED) 18 to a circuit board 10. The LED 18 is supported over a land 12, or conductive terminal, of the circuit board 10 by way of a pad 20 formed from a conductive elastomer. Kepchar does not teach or suggest that land 12 and pad 20 form a single conductive element.

The remainder of the structure depicted in FIG. 1 of Kepchar forms a so-called "light pipe" 30 for the LED 18. That structure includes a thin conductive coating 26 that communicates directly with the LED 18 and with another land 14 of the circuit board 10 by way of a pad 22, which, like pad 20, is formed from a conductive elastomer. The thin conductive coating 26 is supported by a plate 24, which is formed from transparent material and permits light to enter the light pipe 30, which is positioned over the LED 18.

It is respectfully submitted that one of ordinary skill in the art would not have been motivated to have modified the teachings of Kepchar in the manner that has been asserted in the outstanding Office Action. Specifically, Kepchar does include any description with respect to conductive traces on the circuit board 10, the LED 18, or the light pipe 30-carrying structure. Coupled with the failure of Kepchar to teach or suggest any conductive structures that include multiple layers, it is quite apparent that one of ordinary skill in the art would not have been motivated to have modified the teachings of Kepchar in such a way as to develop a conductive trace that is at least partially carried by a semiconductor device component and that includes a plurality of superimposed, contiguous, mutually adhered layers.

It is also respectfully submitted that Kepchar does not teach or suggest each and every element of any of claims 47-68 or 75-90 of the above-referenced application.

Independent claim 47, as amended and presented herein, recites a conductive trace that is at least partially formed on at least one semiconductor device component and that

comprises a plurality of superimposed, contiguous, mutually adhered layers of conductive material.

By way of contrast with independent claim 47, the pads 20 and 22 are not formed at least partially on the circuit board 10, the LED 18, or the structure which supports the light pipe 30. Rather, pad 20 is a structure that is located between land 12 of the circuit board 10 and the LED 18, while pad 22 is a structure that is located between land 14 of the circuit board 10 and the conductive coating 26 on the transparent plate 24 of the light pipe 30-carrying structure.

Moreover, neither the pads 20, 22 nor the conductive coating 26 on layer 24 are conductive traces, as required by amended independent claim 47.

Accordingly, it is respectfully submitted that Kepchar does not teach or suggest each and every element of independent claim 47.

In view of the foregoing, it is respectfully submitted that a *prima facie* case as to the obviousness of independent claim 47 has not been established under 35 U.S.C. § 103(a).

Each of claims 48-51 is allowable, among other reasons, as depending from claim 47, which is allowable.

Claim 48 is further allowable since Kepchar lacks any teaching or suggestion of a conductive trace that includes a plurality of layers that comprise a thermoplastic conductive elastomer.

Claim 49 is additionally allowable since Kepchar does not teach or suggest a conductive trace with a plurality of layers that comprise metal.

Claim 51 is also allowable because Kepchar lacks any teaching of suggestion of a conductive trace that is configured to at least partially connect two semiconductor device components. Rather, the circuit board 10 and LED 18 of Kepchar are electrically connected by a pad 20, while the light pipe 30-carrying structure and the circuit board 10 are electrically connected by way of another pad 22.

Independent claim 52, as amended and presented herein, recites a semiconductor device that includes a semiconductor device component and at least one conductive trace carried by the

semiconductor device component. The at least one conductive trace of amended claim 52 includes a plurality of superimposed, contiguous, mutually adhered layers comprising conductive material.

In contrast to amended claim 52, Kepchar lacks any teaching or suggestion of a semiconductor device component that carries at least one conductive trace that includes a plurality of superimposed, contiguous, mutually adhered layers. Rather, Kepchar teaches a light-pipe 30-carrying structure that includes a single-layered conductive coating 26 on a transparent layer 24 thereof, as well as small conductive pads 20 and 22 that respectively connect an LED 18 and a land 14 of a circuit board 10 to the conductive coating 26. None of these structures has a plurality of superimposed, contiguous, mutually adhered layers.

Accordingly, it is respectfully submitted that Kepchar does not teach or suggest each and every element of amended independent claim 52.

Each of claims 53-63 is allowable, among other reasons, as depending either directly or indirectly from claim 52, which is allowable.

Claim 55 is additionally allowable because Kepchar does not teach or suggest that a dielectric layer on an active surface of a semiconductor die may carry at least one conductive trace including plurality of superimposed, contiguous, mutually adhered layers.

Claim 56 is further allowable since Kepchar lacks any teaching or suggestion of a semiconductor device including at least one conductive trace with a plurality of layers that comprise a thermoplastic conductive elastomer.

Claim 57 is further allowable since Kepchar neither teaches nor suggests a semiconductor device that includes at least one conductive trace with a plurality of layers that comprise a metal.

Claim 60 is also allowable because Kepchar does not teach or suggest that a conductive trace that has the features recited in claim 52 may be carried by a semiconductor die.

Claim 62 is additionally allowable since Kepchar does not teach or suggest that a conductive trace with the features recited in claim 52 may be carried by a semiconductor device component that comprises leads.

Claim 63, which depends from claim 62, is further allowable because Kepchar lacks any teaching or suggestion of a conductive trace that may contact a lead of a semiconductor device component.

Independent claim 64 recites a semiconductor device assembly that includes a carrier, at least one semiconductor die adjacent to the carrier, and conductive elements that electrically connect contacts of the carrier to corresponding bond pads. Independent claim 64 also recites that each of the conductive elements includes a plurality of superimposed, contiguous, mutually adhered layers comprising conductive material.

It is respectfully submitted that Kepchar does not teach or suggest a semiconductor device assembly of the type recited in claim 64. In particular, Kepchar lacks any teaching or suggestion of an assembly that includes a carrier, at least one semiconductor die adjacent thereto, and conductive elements that electrically connect contacts of the carrier to corresponding bond pads of the at least one semiconductor die. Moreover, Kepchar lacks any teaching or suggestion that such conductive elements may include a plurality of superimposed, contiguous, mutually adhered layers.

Each of claims 65-68 is allowable, among other reasons, as depending from claim 64, which is allowable.

Claim 66 is further allowable since Kepchar neither teaches nor suggests an assembly that includes a carrier that comprises leads.

Claim 67 is additionally allowable because Kepchar does not teach or suggest conductive elements that may be formed from a plurality of layers that comprise a thermoplastic conductive elastomer.

Claim 68 is further allowable since Kepchar lacks any teaching or suggestion of conductive elements that include a plurality of layers that comprise a metal.

Independent claim 75 recites a semiconductor device assembly that includes a first semiconductor device component, a second semiconductor device component, and at least one conductive element connecting at least one contact pad of the first semiconductor device component to at least one contact pad of the second semiconductor device component. In addition, independent claim 75 recites that the at least one conductive element comprises a plurality of superimposed, contiguous, mutually adhered layers.

By way of contrast, Kepchar includes no teaching or suggestion of an assembly that includes a conductive element with a plurality of superimposed, contiguous, mutually adhered layers that connects contact pads of two semiconductor device components. Rather, Kepchar describes a first pad 20 that electrically connects a land 12 of a circuit board 10 to an LED 18 and a second pad 22 that electrically connects another land 14 of the circuit board 10 to a conductive coating 26 of a light pipe 30-carrying structure. Kepchar does not teach or suggest that either the LED 18 or the conductive coating 26 includes or forms a contact pad, as recited in independent claim 75. Moreover, neither pad 20, 22 includes more than one layer, as required by independent claim 75.

Therefore, it is respectfully submitted that Kepchar neither teaches or suggest each and every element of independent claim 75.

Each of claims 76-90 is allowable, among other reasons, as depending either directly or indirectly from claim 75, which is allowable.

Claim 76 is further allowable since Kepchar does not teach or suggest a conductive element that includes a plurality of layers that comprise a conductive elastomer.

Claim 77 is also allowable since Kepchar lacks any teaching or suggestion of a conductive element that includes a plurality of layers that comprise a metal.

Claim 79 is further allowable since Kepchar does not teach or suggest that any of the circuit board 10, LED 18, or the light pipe 30-carrying structure thereof is a packaged semiconductor die.

Claim 80 is additionally allowable since Kepchar includes no teaching or suggestion of an assembly of which both the first and second semiconductor devices comprise at least one semiconductor die. It is respectfully submitted that neither the circuit board 10 nor the light pipe 30-carrying structure of Kepchar comprises a semiconductor die.

Claim 85 is further allowable because Kepchar lacks any teaching or suggestion of a conductive element that extends across a peripheral edge of at least one of a first semiconductor device component and a second semiconductor device component.

Claim 86, which depends from claim 80, is further allowable since Kepchar does not teach or suggest an assembly that includes a carrier substrate upon which at least one of the at least two semiconductor dice is disposed.

Claim 87, which depends from claim 86, is also allowable since Kepchar includes no teaching or suggestion of an assembly that includes at least one other conductive element that connects another contact pad of one of the at least two semiconductor dice to a contact pad of the carrier substrate.

Claim 88 depends from claim 87 and further recites that the at least one other conductive element includes a plurality of superimposed, contiguous, mutually adhered layers comprising conductive material, elements which are neither taught nor suggested by Kepchar.

Claim 89, which depends from claim 88, is additionally allowable since Kepchar does not teach or suggest a multi-layered conductive element having layers that are formed from a conductive elastomer.

Claim 90, which depends from claim 88, is additionally allowable because Kepchar does not teach or suggest a conductive structure that includes a plurality of contiguous layers that comprise a metal.

In view of the foregoing, it is respectfully submitted that Kepchar does not render obvious any of claims 45-68 or 75-90 of the above-referenced application under 35 U.S.C. §

103(a). Accordingly, it is respectfully requested that the section 103(a) rejection of each of these claims be withdrawn.

Hata

Claims 47-68 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 4,891,635 Hata (hereinafter "Hata").

Hata teaches an electrostatic display element. The electrostatic display element of Hata includes two spaced apart electrodes 1 and 2 having interior surfaces that face one another and which are lined with insulative layers 15 and 25 that have different colors from each other. A flexible, central electrode 3 is positioned between the first and second electrodes 1 and 2 and includes a flexible, thin dielectric film 31 which has surfaces that are coated with conductive layers 32 and 33. It is clear from FIGs. 1 and 3(b) of Hata that the central electrode 3 is a planar member.

It is respectfully submitted that one of ordinary skill in the art would not have been motivated to modify the teachings of Hata in the manner that has been suggested in the outstanding Office Action. In particular, with respect to claims 47-63, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to modify the teachings of Hata in such a way as to develop a conductive trace that is at partially formed on at least one semiconductor device component, as the central electrode 3 is a planar member that is not formed on a semiconductor device component. With respect to claims 64-68, it is respectfully submitted that one ordinary skill in the art would not have been motivated by the teachings of Hata, which are limited to the electrostatic display element, to come up with an assembly that includes a carrier, at least one semicondcutor die, and conductive elements that connect contact pads of the carrier to bond pads of the at least one semiconductor die.

In addition, it is respectfully submitted that Hata does not teach or suggest each and every element of any of claims 47-68.

Independent claim 47, as amended and presented herein, recites a conductive trace that includes a plurality of superimposed, contiguous, mutually adhered layers, each of which comprises conductive material.

The only elements described in Hata that are remotely similar to the conductive trace of amended claim 47 are the central electrode 3 and the assembly of the central electrode with contact plates 52 and 53.

The central electrode 3 includes a dielectric film 31 sandwiched between two conductive layers 32 and 33. Thus, the two conductive layers 32 and 33 of the central electrode 3 are not contiguous with one another, as required by amended claim 47.

Furthermore, the contact plates 52 and 53 described in Hata are mechanically secured to one another by way of screws 71 and 72 that cause first and second electrodes 1 and 2 to be biased against one another and, thus, to force each of the elements therebetween against one another. Therefore, the contact plates 52 and 53 are not mutually adhered, as required by independent claim 47. Nor, for the same reason, is either contact plate 52, 53 adhered to the adjacent conductive layer 32, 33.

Claims 48-51 are each allowable, among other reasons, as depending from claim 47, which is allowable.

Claim 51 is additionally allowable since Hata neither teaches nor suggests that the central electrode 3 of the electrostatic display device described therein or the assembly of the central electrode 3 with contact plates 52 and 53 is configured to electrically connect two semiconductor device components.

Independent claim 52, as amended and presented herein, recites a semiconductor device that includes a semiconductor device component and at least one conductive trace carried by the semiconductor device component. The at least one conductive trace of independent claim 52 includes a plurality of superimposed, contiguous, mutually adhered layers, each of which comprises conductive material.

Again, Hata neither teaches nor suggests that the central electrode 3 thereof includes a plurality of layers that comprise conductive material and that are contiguous with one another. Rather, conductive layers 32 and 33 are separated from one another by way of a thin dielectric film 31.

Also, Hata does not teach or suggest that the contact plates 52 and 53 that secure the central electrode in place are mutually adhered to one another or to the adjacent conductive layers 32 and 33, respectively, of the central electrode. Instead, contact plates 52 and 53 are held against one another and against the conductive layers 32 and 33 of the central electrode 3 by the forces acting thereon as screws 71 and 72 cause electrodes 1 and 2 to be biased toward one another.

For these reasons, it is respectfully submitted that Hata does not teach or suggest each and every element of independent claim 52, as is required to maintain a rejection under 35 U.S.C. § 103(a).

Each of claims 53-63 is allowable, among other reasons, as depending from claim 63, which is allowable.

In addition, claim 55 is allowable because Hata neither teaches nor suggests that either the central electrode 3 thereof nor the assembly of the contact plates 52 and 53 and the central electrode is carried by a dielectric layer disposed on an active surface of a semiconductor die.

Claim 60 is further allowable since Hata does not teach or suggest that either the central electrode 3 or the assembly of the contact plates 52 and 53 and the central electrode 3 communicates with a contact of a semiconductor die.

Claim 61 is also allowable since Hata includes no teaching or suggestion that the central electrode 3 or the contact plate 52, 53-central electrode 3 assembly is carried by a packaged semiconductor device.

Independent claim 64 recites a semiconductor device assembly that includes, among other things, a carrier and at least one semiconductor die adjacent to the carrier. Independent claim 64

also recites that conductive elements connect bond pads of the at least one semiconductor die to corresponding contacts of the carrier.

Hata lacks any teaching or suggestion of an assembly that includes a carrier and a semiconductor die. In addition, Hata does not teach or suggest that any conductive structure thereof would be useful for connecting a bond pad of a semiconductor die to a contact of a carrier.

Moreover, Hata does not teach or suggest that either the central electrode 3 thereof or the assembly of the central electrode 3 with contact plates 52 and 53 forms a conductive element with a plurality of contiguous layers that comprise conductive material and that are mutually adhered to one another. Rather, the conductive layers 32 and 33 of the central electrode 3 are spaced apart from one another by way of a dielectric film 31 and, thus, are not contiguous, while the contact plates 52 and 53 are secured to one another and to adjacent conductive layers 32 and 33 of the central electrode by way of compressive forces, not mutual adhesion.

Accordingly, it is respectfully submitted that Hata does not teach or suggest each and every element of independent claim 64 and, therefore, does not render the subject matter recited in independent claim 64 obvious under 35 U.S.C. § 103(a).

Claims 65-68 are each allowable, among other reasons, as depending from claim 64, which is allowable.

In view of the foregoing, it is respectfully submitted that, under 35 U.S.C. § 103(a), each of claims 47-68 is allowable over Hata and, therefore, requested that the section 103(a) rejections of these claims as being rendered obvious by Hata be withdrawn.

CONCLUSION

It is respectfully submitted that each of claims 47-68 and 75-90 is allowable. An early indication of the allowability of each of these claims is respectfully solicited, as is a notice that the above-referenced application has been passed for issuance. If any issues preventing the allowance of any of claims 47-68 or 75-90 remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,

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Enclosure: Version with Markings to Show Changes Made
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

47. (Amended) A conductive [element] trace at least partially formed on at least one semiconductor device component, comprising a plurality of superimposed, contiguous, mutually adhered layers, each of said layers comprising [of] conductive material.

48. (Amended) The conductive [element] trace of claim 47, wherein said conductive material comprises a thermoplastic conductive elastomer.

49. (Amended) The conductive [element] trace of claim 47, wherein said conductive material comprises a metal.

50. (Amended) The conductive [element] trace of claim 47, configured to be carried by a single semiconductor device component.

51. (Amended) The conductive [element] trace of claim 47, configured to at least partially electrically connect two semiconductor device components.

52. (Twice Amended) A semiconductor device comprising:

a semiconductor device component; and

at least one conductive [element] trace carried by said semiconductor device component, said at least one conductive [element] trace including a plurality of superimposed, contiguous, mutually adhered layers, each of said layers comprising conductive material.

53. (Amended) The semiconductor device of claim 52, wherein said at least one conductive [element] trace is substantially entirely carried by said semiconductor device component.

58. (Amended) The semiconductor device of claim 52, wherein said at least one conductive [element] trace communicates with a contact of said semiconductor device component.

64. (Amended) A semiconductor device assembly, comprising:

a carrier; and

at least one semiconductor die adjacent said carrier, said semiconductor die including bond pads; and

conductive elements electrically connecting contacts of said carrier to corresponding bond pads, each of said conductive elements including a plurality of superimposed, contiguous, mutually adhered layers, each of said layers comprising conductive material.